said charge source layer comprises a thin layer of P+ type material.

35. A semiconductor imaging device of according to claim 33, wherein:

said cladding layer comprises a layer of P type material.

Cont B5

36. A semiconductor imaging device according to claim 26, wherein:

said multilayer sandwich is substantially formed from group III-V materials.

REMARKS

The Examiner has objected to the specification under 35 U.S.C. 112, first paragraph and 37 CFR 1.71. Applicant has amended the specification and the drawings to address the objections identified by the Examiner. Note that large number of paragraphs added to the end of the specification correspond to the original claims and abstract as filed in this patent application. It is respectfully submitted that no new matter has been added.

The Examiner has rejected claims 9-24 under 35 U.S.C. Section 112, first paragraph. According to the Examiner, the structure of the semiconductor imaging device (claim 9), the three phase

clocking scheme (claim 22) and the active pixel image sensor (claim 24) are not clearly described to enable any person skilled in the art to make and use the invention. Applicant respectfully traverses the Examiner's rejection for the following reasons.

With respect to claim 9, Applicant respectfully submits that the structure and operation of the semiconductor imaging device of claim 9 are provided in detail in the specification (page 8, line 9 to page 9, line 20 and page 12 to page 18).

With respect to claim 22, Applicant respectfully submits that the operation of the three phase clocking scheme is well known in the art as evidenced by Fig. 10 and the accompanying text on page 6 of the article entitled "Kodak CCD Primer, #KCP-001, Charge Coupled Device (CCD) Image Sensors", distributed by the Eastman Kodak Company and attached hereto. However, in order to advance prosecution, Applicant has elected to cancel claim 22 and hereby reserves the right to pursue such subject matter in a continuation application.

With respect to claim 24, Applicant has amended claim 24 to more clearly define the invention claimed therein. Such recitations are clearly supported by pages 12 to page 18 of the substitute specification provided herein.

With respect the Figures, Applicant respectfully submits that Figs. 2, 2a, 3 and 4 clearly describe imaging applications of the multilayer structure of Fig. 1 as recited in the claims.

New claims 25-36 have been added. It is respectfully submitted that the new claims are supported by the specification, and are allowable over the prior art.

In light of all of the above, it is submitted that the claims are in order for allowance, and prompt allowance is earnestly requested. Should any issues remain outstanding, the Examiner is invited to call the undersigned attorney of record so that the case may proceed expeditiously to allowance.

Respectfully submitted,

David P. Gordon

David P. Gordon
Reg. #29,996
Attorney for Applicant(s)

65 Woods End Road
Stamford, CT 06905
(203) 329-1160
September 26, 2002

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resonant cavity at the wavelength of interest in the LWIR or MWIR regions. In the described embodiment, ion implants are used for several purposes. The N type implant is used to form source and drain regions to the inversion channel, and it is also used to shift the threshold voltage of the inversion channel interface. The epitaxial structure is grown as a normally off (enhancement) device and then the N type implant is used to create regions of normally on (depletion) devices and it is these regions where the charge packets are stored. Oxygen implants may also be used to create high resistance regions below the implants. The technology utilizes the oxidation of AlAs and other layers with large aluminum percentages to achieve passivation, isolation and dielectric mirrors below the structure.

The basic structure of the pixel and the output amplifiers which are employed in the CCD may also be used to design an active pixel sensor. In such a design, each pixel is interfaced to an output amplifier and a row or a column is output in parallel.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a schematic view of the epitaxial layer structure indicating the modulation doped interface, the delta-doped resistively coupled layer and the delta-doped p contact layer

FIG.2 is a fabricated device cross-section of the CCD pixels including the pixel storage region, the pixel blocking region and the inter-pixel transfer region.

FIG. 2a is the potential profile of the device of Fig. 2.

FIG.3 is an energy diagram cross-section in the vertical direction through a storage pixel in the illuminated condition showing all of the significant current flows from the contacts and into and out of the well.

FIG.4 is schematic drawing of the last storage well in the CCD and its connection by way of a separate clocked output gate to the output differential amplifier by way of a floating diffusion node which is reset each clock cycle. For the active pixel, Vϕ is the single storage element connected to the output stage.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG.1 shows the epitaxial layer structure corresponding to the preferred embodiment and from which the CCD, the active pixel and the HFET (heterostructure field effect transistor) can be made. The layer structure starts from a semi-insulating GaAs substrate 100 and grows a DBR (distributed Bragg reflector) mirror stack of 1 - 3 pairs of 1/4 wavelength mirror using combinations of GaAs as layer 152 [151] and AlAs as layers 151 [152] which are subsequently oxidized to produce layers of AlxOy positioned between layers of GaAs. These layers form a bottom mirror for a cavity which is resonant at the intersubband wavelength of interest. Only a few pairs are used (1 - 3) to create a modest resonance in order to limit the total layer thickness and therefore epitaxial growth time. Following the DBR growth, a layer 170 of p+ GaAs of about 0.5μm is grown to enable a bottom ohmic contact to the collector electrode 170A. Then a layer 171 of $Al_{x1}Ga_{y1}As$ ($0.4< x1<1$), and where $y1=1-x1$) is grown to a thickness of about 1000-2000 Å to assist in the contact formation with a p type doping of about $10^{18}cm^{-3}$.and is followed by another layer 156 of undoped $Al_{x1}Ga_{y1}As$ of about 1000-3000 Å to provide carrier confinement. This is followed by layer 157 of undoped $Al_{x2}Ga_{y2}As$ ($0.1 < x2 < 0.3$) and then a separation layer 158 of undoped GaAs. Layer 158 enables a growth interruption to lower the

growth temperature for growing the quantum well(s). Layers 157 and 158 isolate the quantum wells from the carrier confinement layers 156. Next the undoped quantum well 160 and and undoped barrier layer 159 are grown as a pair and there may be one to three pairs. The quantum well has been designed for intersubband absorption. A thin layer 161 of undoped GaAs of about 30 Å is then grown as a spacer which enables a growth temperature change between the InGaAs well and the layers above the well(s). The GaAs spacer is followed by an undoped spacer layer 162 of about 30 Å of $Al_{x2}Ga_{y2}As$. Then the modulation doped layer 163 of N+ type doped Al $_{x2}Ga_{y2}As$ (where y2 = 1 - x2) is grown with a thickness of 40-100Å to contain an ion density of $10^{12}cm^{-2} < Q < 4x10^{12}cm^{-2}$. On top of the modulation doped layer is grown an undoped capacitor spacer layer 164 of 100-300 Å thickness which can be as thin as possible consistent with the growth and fabrication. On top of the capacitor layer is grown a P+ doped layer 165 which serves as the charge source layer for the gate. This layer should be as thin as possible and as highly doped as possible providing that it remains only partially depleted under all conditions of operation, i.e. a portion of this layer, however small, always remains undepleted. Above the charge source layer is grown a cladding layer 166 of thickness 500 Å < z <2000 Å, of doping in the range of $10^{17}cm^{-3}$ and of composition $Al_{x1}Ga_{y1}As$. This layer serves to block minority carrier injection into the gate. The final layer 167 is a GaAs layer of about 100 Å or thinner and with P++ type doping which enables the formation of a very low resistance ohmic contact for hole carriers to the gate electrode 120.

The CCD is formed as a series of mesas 115 in Fig.2 and referred to as pixels, separated by regions 116 referred to as the inter-electrode transfer regions in Fig.2 . The mesas are created by patterning the original wafer (with photoresist for example) and then etching (typically by reactive ion etching for accuracy) to the charge source layer 165. Between the electrodes, an ion implant 121 is positioned so that the storage region 118 and the adjacent barrier region 117 of the next mesa are connected by a high conductivity region. This implant 121 is simultaneously used

to form the source and drain regions of all transistors in the integrated circuit. Thus each storage region is connected to the next barrier region by a source implant. These inter-electrode regions are designed to maximize the drift current from pixel to pixel during charge transfer. Suppose that the voltage difference between clock phases is 2V and it is desired to achieve the maximum channel velocity corresponding to $E=5x10^3$ V/cm. Then an inter-electrode region width of 4 μm would be desirable. The pixels are divided into a barrier region 117 and a storage region 118. The barrier region is contacted by the metal gate electrode 120 which is formed from a refractory metal such as tungsten or a tungsten alloy and produces an ohmic contact with the topmost GaAs layer 167. The gate electrode 120 is formed upon the as-grown epitaxial material which has an enhancement threshold meaning that it is in the off condition with zero gate voltage. The storage region is adjacent to the barrier region and is defined with an ion implant 119 of N type species into the active layer. Therefore, the region of the mesa without the implant, defines the barrier region. The purpose of the implant is to move the threshold of the interface to a normally on condition so that the potential profile under the gate electrode appears as shown in Fig. 2a. The metal emitter (gate electrode 120) is patterned to be approximately positioned over the barrier portion and to be equal to or greater than the barrier length. It is self-aligned to the left edge of the mesa. However, the P++ GaAs layer 167 is low enough in resistance to force the entire surface of the mesa to be at the potential of the metal electrode for all the current densities of interest in the operation. The storage section of the pixel is therefore at a constant potential along its length y in Fig.2 and this means the storage section is an equipotential region. The operation of this CCD is 1 1/2 phase which means that alternate electrodes are clocked to a voltage V_ϕ and the other electrodes are held at a dc potential V_{dc}. The potential profiles under the clocked electrode and the dc electrode are shown in Fig. 2a, which illustrates the transfer mechanism. The voltage difference $\Delta V = V_\phi - V_{dc}$ is applied to the resistor consisting of the P+ layer 165 between the mesas (i.e., in the inter-electrode region). The length of the resistor is chosen to maximize the velocity in the interelectrode transfer region. The maximum velocity

therefore maximizes the current flow which is given by J=qvn, where v is the carrier velocity, q is the electronic charge and n is the carrier density. To optimize the transfer efficiency, it is necessary to maximize the current flow. This is achieved with the maximum value of v and the maximum value of n. The maximum value of v is obtained as just discussed and the maximum value of n is obtained by the implanted N+ region between electrodes as discussed above.

The scheme just discussed is a 1 1/2 phase clocking scheme. As is well known in Si technology, there are many possible clocking schemes and these may also be implemented here. These include a) a three phase clocking scheme wherein the pixels are grouped into sets of three ordered pixels, the first pixel in each set is clocked with a phase I clock, the second pixel in each set is clocked with a phase II clock and the third pixel in each set is clocked with a phase III clock [every third pixel is clocked with a phase I clock, the adjacent pixels to every third pixel are clocked with a phase II clock and the remaining pixels are clocked with a phase III clock], b) a fully two phase clocking scheme wherein every other pixel is clocked with a phase I clock and the remaining pixels are clocked with a phase II clock, and c) a uni-phase clocking scheme. The uni-phase clocking scheme is usually referred to as a virtual phase CCD and is achieved with a series of strategically placed p and n implants. The uni-phase operation has been exploited successfully in Si CCD's which use a buried electron channel to store the charge. The surface of the buried channel is inverted by voltage to produce a hole inversion channel which clamps the potential of the electron channel. This natural clamping of the surface potential by the formation of a p channel eliminates the need for a separate dc electrode allowing a single electrode to be used. The voltage at which this clamping occurs is controlled locally with a p type implant. All of these clocking schemes are applicable to the Inversion Channel GaAs CCD.

The CCD described above has the unique capability of detecting an input signal in the spectral range from about 3μm to 20μm by the mechanism of intersubband absorption. The

energy band diagram of the device is shown in Fig.3 . It shows the quantum well and the current flows of charge carriers which may either fill the well or empty the well. The current flows into the well are the thermal emission from the modulation doped layer 163 [161] to the left of the well, and the generation currents flowing toward the well(s) from the collector depletion layer consisting of the layers 170, 171,156, and 157 and from the quantum well(s) and barrier(s) which are layers 159 and 160 respectively. The currents flowing out of the well are the thermal emission current from the quantum well into the modulation doped layer 163 and the photocurrent from the quantum well into the modulation doped layer produced by the intersubband absorption in the quantum well. The other important current flow is the recombination current Jrb which allows electrons to flow from the modulation doped layer to the emitter contact (metal gate electrode 120) via electron-hole recombination current in the capacitor layer 164. During the operation as a photodetector, the gate electrode 120 [emitter] is forward biased with respect to the collector contact layer 170/collector electrode 170A [collector (156, 157, 170, 171)]. This means that the capacitor layer 164 is forward biased and the collector contact layer 170 is reverse biased which enables the photocurrent to be conducted out of the system by forward bias and the dark current current flow (Jrbd) in the system to be controlled by the reverse bias across the collector contact layer 170. The operation of the photodetector is described as follows. The quantum well is initially filled substantially in the absence of light. A reasonable design is that the Fermi energy is above the first subband in the quantum well. Then the absorption will be maximized because it is proportional to the number of electrons in the initial state. When long wavelength light is incident, then the photocurrent empties the quantum well. The dark current flowing into the well is produced by the generation current which is produced by emission across the energy gap of the quantum well or the barrier regions. The noise current in in the device which represents the limit to the detectable power is specified by the dark current Id and it is where q is the electronic charge and B is the bandwidth. In a conventional QWIP device, the dark current flows over a small barrier of a size comparable to the quantum

well and therefore to obtain high background limited operation , it is necessary to cool the device to cryogenic temperatures of 50-60K in order to reduce Id. Only at these temperatures can the shot noise associated with the dark current be reduced to a level that is comparable to the noise associated with the black body radiation from the scene at a temperature of 300K.

The structure illustrated in Figs. 1-3 has a fundamental advantage in reducing the dark current flow even at temperatures up to and above 300K. The reason is that the barrier to the generation of dark current and the barrier to the optical emission from the quantum well are distinctly different. As the diagram shows, the dark current is produced by the thermal emission across the energy gap of either the quantum well (corresponding to strained InGaAs with a bandgap of about 1.24eV), the barrier region (corresponding to GaAs with a bandgap of 1.42eV), and the depletion regions (corresponding to $Al_{x2}Ga_{y2}As$ with a bandgap of 1.65eV). Generally speaking the depletion regions become the main source of dark current. In contrast to the dark current barrier, the optical emission barrier is the energy interval between the first subband in the quantum well and the top of the well (this is basically the depth of the quantum well). Because this structure has decoupled the dark current generation barrier from the optical emission barrier, then it is possible to operate at room temperature and still achieve BLIP operation. Therefore we may realize all of the benefits of high resolution and high speed photovoltaic sensing offered by the QWIP detection mechanism with an uncooled semiconductor chip.

The infrared detection mechanism described above has been described as an integral part of an efficient CCD structure in GaAs. However the detector could equally as well be incorporated into the photo-sensitive portion of an active pixel structure. In the active pixel , the charge is transferred across one barrier to a bit line which connects to the sense amplifier. The charge transfer mechanisms are identical to those of the CCD, but the charge transfer efficiency is much less of an issue because there is only one transfer gate separating the storage area from the sensing node. The tradeoff is that the fill factor of the active pixel is less than the CCD because

more circuitry is required. Therefore the operation of the intersubband detector is identical in the CCD and active pixel architectures.

In both the CCD and the active pixel devices, the signal of interest is actually the the charge that is removed from the well. For very weak optical input signals, very little charge is removed and for very strong optical inputs the well is essentially emptied at the end of the imaging cycle. The situation is ideal for the elimination of noise in the detection process because it requires differential operation to obtain the actual output signal. For example, if the output of the imaged pixel is input to one side of a differential amplifier, then it is appropriate to input a signal to the other side of the DA from a full well to perform as a reference level. These connections are illustrated in Fig.4 which shows a storage gate V_{ϕ}, a transfer gate V_{dc}, a reset gate V_{reset}, a differential amplifier and two reference nodes, one for a full well and one for an empty well. This situation is identical to that used in the correlated double sampling scheme in advanced CCD read-out circuits to reduce set:reset noise. There are several noise mechanisms contributing noise to the amplifier inputs which include clocking noise, kTC noise on the reset transistor, and shot noise on the dark current to mention a few. All of the noise mechanisms that are common to the read-out of the cell with and without data, are reduced by the common mode rejection ratio of the differential amplifier. Therefore the intersubband detection within the inversion channel has a fundamental advantage because the differential process is essential to recover the signal, and yet at the same time, it performs the role of reducing many noise mechanisms according to the differential rejection of common mode signals.

In accordance with the present invention, a semiconductor imaging device is provided that is comprised of the following layer structure:

a distributed bragg reflector mirror epitaxially grown upon a semiinsulating GaAs substrate;

a first layer of P+ type GaAs deposited on said epitaxial mirror;

a layer of P+ type aluminum gallium arsenide (70%Al) disposed on said layer of GaAs;

a layer of P type aluminum gallium arsenide (70%Al) disposed on said layer of P+ type aluminum gallium arsenide;

a Pseudomorphic High Electron Mobility Transistor (PHEMT) transistor epitaxial layer structure without a schottky contact and using N type modulation doping, disposed on said layer of P type aluminum gallium arsenide, said PHEMT epitaxial layer structure comprising a layer of aluminum gallium arsenide (15%Al), a layer of GaAs, one to three quantum wells of strained InGaAs separated by GaAs barriers, a spacer layer of aluminum gallium arsenide (15%Al), a modulation doped layer of aluminum gallium arsenide (15%Al) and a gate spacer layer of aluminum gallium arsenide (15%Al) ;

a planar doped layer of P+ type aluminum gallium arsenide (15%Al) disposed on said PHEMT epitaxial layer structure;

a cladding layer of aluminum gallium arsenide (70%Al) of modest P type doping disposed on said planar doped layer; and

a layer of GaAs of P++ type doping disposed on said cladding layer.

In addition, a charge coupled device (CCD) may be realized with the epitaxial growth structure summarized above. The CCD comprises a linear array of mesas in which charge may be stored and transferred from one mesa to the next by a suitable arrangement of clock pulses applied to said mesas, said linear array being terminated in a charge sensitive amplifier for the purposes of detection of said stored charge when transferred to said amplifier, said mesas being adjacent to each other and separated by transfer regions which have been etched from the original surface to the top of a lower P+ planar-doped layer, said transfer regions being implanted with N+ type doping to form a low resistance path between said mesas thereby enabling high efficiency transfer; each pixel being comprised of a barrier section and a storage section, said

barrier section being defined by a refractory metal top electrode which results in an enhancement transistor threshold in said barrier regions, and said barrier region being connected electrically by an uppermost p+ charge sheet to said storage region to maintain an equipotential across said mesa, said storage region forming an optical aperture with no metal top contact and being shifted electrically in threshold by an ion implant resulting in a depletion transistor in said storage region, said storage region being contained in a vertical optical cavity, said cavity being terminated in the vertical direction on its top surface by a deposited DBR mirror and on its bottom by a grown epitaxial mirror so that resonant absorption may occur in said cavity formed by said mirrors for light admitted to the structure from either the top or the bottom of said cavity.

A single pixel may be associated with each output charge detection and amplification stage. This configuration, defined as an active pixel structure, has the advantage over a CCD of a minimum loss corresponding to a single transfer to an dedicated output charge sensitive amplifier to that pixel and having the disadvantage of a larger area per pixel resulting from said dedicated amplifier.

Every other pixel of the CCD may be biased to a constant voltage and the remaining pixels are clocked with a single phase clock to produce 1 1/2 phase operation.

Altermately, every other pixel may be clocked with a phase I clock and the remaining pixels are clocked with a phase II clock to produce 2 phase operation.

In another configuration, the pixels are grouped into sets of three ordered pixels, and the first pixel in each set is clocked with a phase I clock, the second pixel in each set is clocked with a phase II clock and the third pixel in each set is clocked with a phase III clock to produce 3 phase operation..

The CCD may have implants placed strategically to obtain uniphase operation

The CCD may operate as follows: the quantum well absorbs input radiation by an intersubband absorption mechanism and wherein said absorption is enhanced by the resonance of a cavity containing said storage region, said input radiation causing electrons residing in a substantially populated well to be emitted from a bound quantum well state into a quasi-bound state at the top of said quantum well or into a continuum of states energetically above said quantum well and to be conducted by thermionic emission, drift and diffusion processes into a gate capacitor section positioned immediately above said quantum well, said emitted electrons producing a deficiency of electrons in said quantum well, said deficiency representing a disturbance from thermal equilibrium which can only be restored by the addition of electrons to said well via the thermal generation of electrons across the bandgap of the host material which is large enough to inhibit dark current flow to such small levels that background limited operation may be obtained in the temperature region around room temperature thereby eliminating the need for cryogenic cooling procedures, said deficiency of charge being detected at a charge amplifier output stage of a CCD array or of a single active pixel stage, said amplifier stage consisting of a floating gate correlated CCD double sampler or a floating diffusion output node with a reset gate capability with the output in either case connected to a differential amplifier such that the electronic output signal from said amplifier represents the difference between a full well of charge and the amount of charge actually transferred from said imaged pixel, said difference signal being reduced in noise content compared to the noise existing on said actual pixel charge.

In accordance with the present invention , a photon detector is realized by using the intersubband absorption mechanism in a modulation doped quantum well(s). The modulation doping creates a very high electric field in the well which enables absorption of input TE

polarized light and also conducts the carriers emitted from the well into the modulation doped layer from where they may recombine with carriers from the gate contact. Carriers are resupplied to the well by the generation of electrons across the energy gap of the quantum well material. The absorption is enhanced by the use of a resonant cavity in which the quantum well(s) are placed. The absorption and emission from the well creates a deficiency of charge in the quantum well proportional to the intensity of the input photon signal. The quantity of charge in the quantum well of each detector is converted to an output voltage by transferring the charge to the gate of an output amplifier. The detectors are arranged in the form of a 2D array with an output amplifier associated with the entire array or a row of the array as in the known charge coupled devices, or a separate amplifier could be dedicated to each pixel as in the known architecture of the active pixel device. This detector has the unique advantage of near room temperature operation because the dark current is limited to the generation across the semiconductor bandgap and not the emission over the quantum well barrier. The detector also has the advantage that the readout circuitry is implemented monolithically by the HFETs formed in the GaAs substrate simultaneously, with the detecting elements.

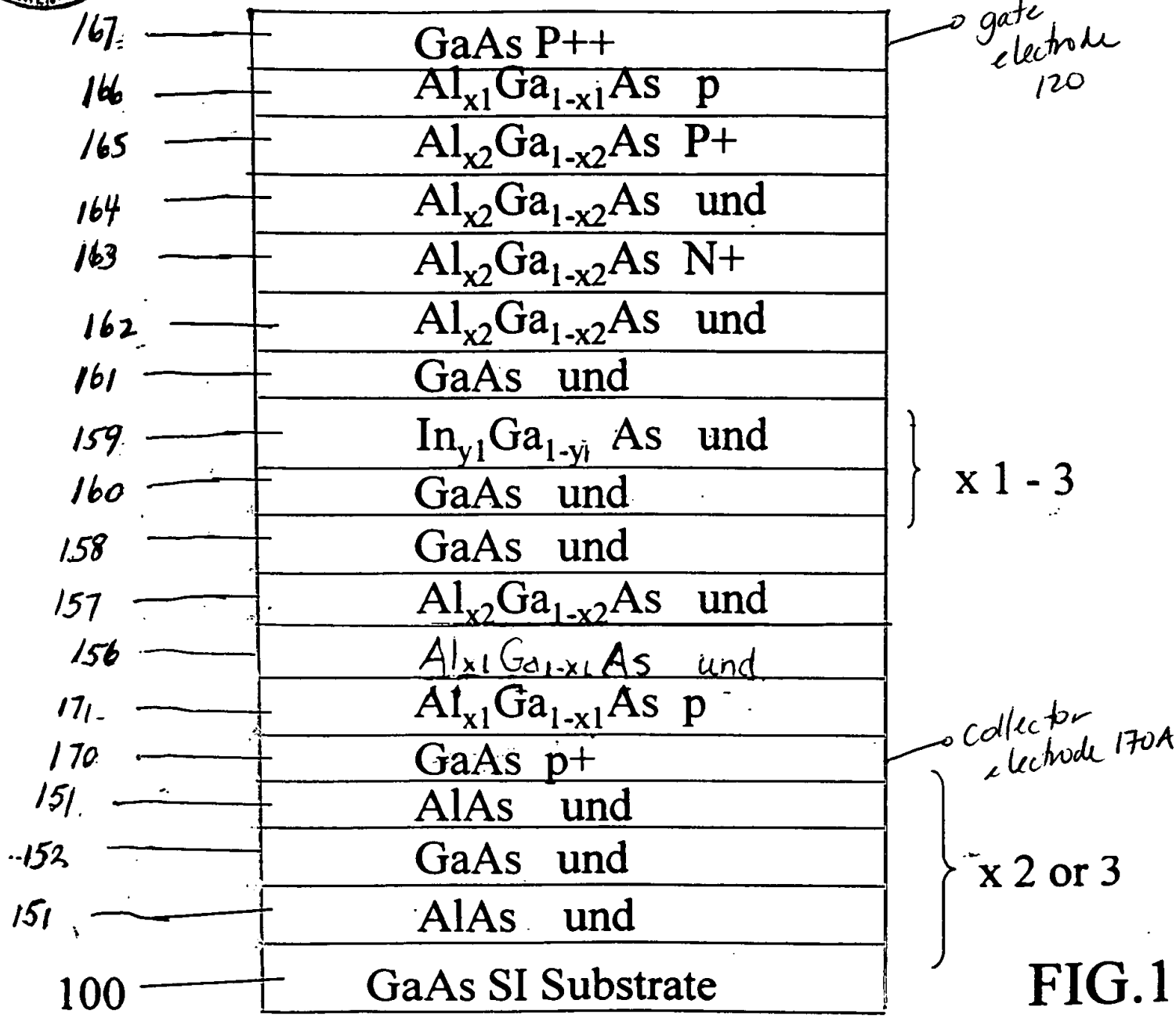

FIG.1

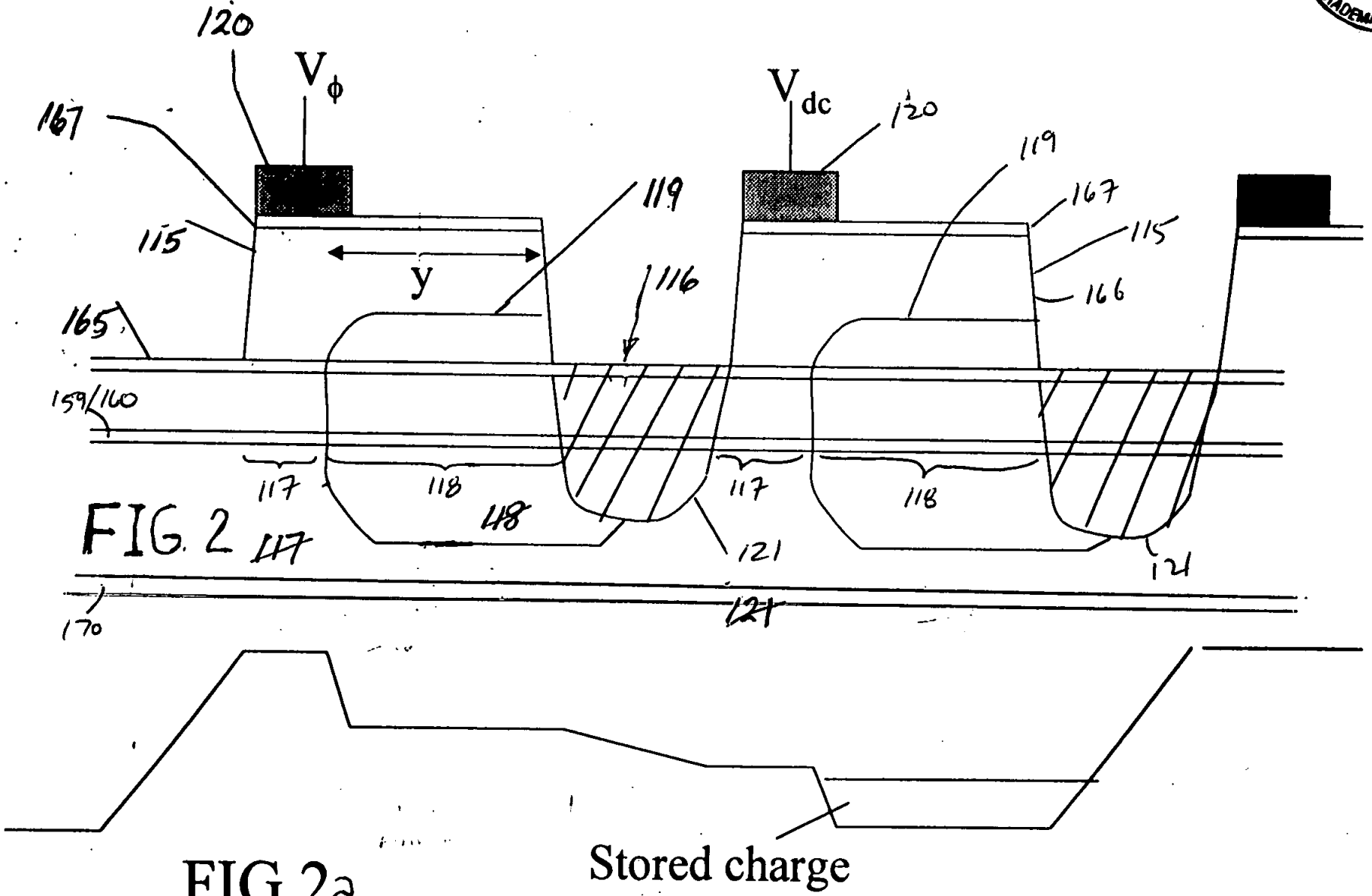

FIG. 2

FIG.2a